WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor device, comprising the steps of:

(i) depositing a sacrificial layer on a substrate having a circuit formed thereon;

(ii) etching the sacrificial layer except for a portion where air gaps are to be formed;

(iii) depositing a low-dielectric layer over the substrate until the portion for air gaps is entirely enclosed in the low-dielectric layer;

(iv) etching the low-dielectric layer to form vias and trenches therethrough;

(v) prior or subsequent to step (iv), removing the portion for air gaps of the sacrificial layer; and

(vi) depositing copper in the vias and trenches which are filled with the copper contacting a surface of the substrate.

2. The method according to Claim 1, wherein step (v) is conducted after step (iv).

3. The method according to Claim 1, wherein step (iii) comprises:

depositing a first low-dielectric layer over the substrate until the first low-dielectric layer and the portion for air gaps are of equal height; and

depositing a second low-dielectric layer on the first low-dielectric layer and the portion for air gaps.

4. The method according to Claim 3, further comprising deposing an etch stop layer between the first low-dielectric layer and the second low-dielectric layer.

5. The method according to Claim 1, wherein the substrate further includes a cap layer on which the sacrificial layer deposits, wherein step (ii) further includes etching the cap layer.

6. The method according to Claim 5, wherein the substrate further includes a wiring layer underneath the cap layer, wherein the wiring layer is connected to the copper.

7. The method according to Claim 1, wherein the sacrificial layer is made of an organic polymer.

8. The method according to Claim 7, wherein the organic polymer is benzocyclobutene (BCB).

9. The method according to Claim 1, wherein step (v) is selective etching based on etching temperature.

10. The method according to Claim 9, wherein the etching temperature is 400°C or lower.

11. The method according to Claim 3, wherein the first low-dielectric layer has a dielectric constant of 3.0 or less.

12. The method according to Claim 11, wherein the first low-dielectric layer has compressive stress.

13. The method according to Claim 3, wherein the first low-dielectric layer is deposited by a combination of dimethyldimethoxysilane (DMDMOS) with divinyldimethylsilane (DVDMS) or oxygen-containg molecules.

14. The method according to Claim 3, wherein the second low-dielectric layer has a dielectric constant of 2.6 or less.

15. The method according to Claim 14, wherein the second low-dielectric layer has compressive stress.

16. The method according to Claim 3, wherein the second low-dielectric layer is deposited by a combination of dimethyldimethoxysilane (DMDMOS) with divinyldimethylsilane (DVDMS) or oxygen-containg molecules.

17. The method according to Claim 1, wherein the portion of air gaps in the low-dielectric layer is formed to give a porosity of 6% to 25%.

18. The method according to Claim 1, wherein the height of the portion for air gaps is in the range of 1nm to 100nm.

19. The method according to Claim 1, wherein the low-dielectric layer including the air gaps has a dielectric constant of 2.3 or less.

20. The method according to Claim 1, which is conducted using a plasma CVD chamber.

21. The method according to Claim 1, wherein the vias and the air gaps are substantially of equal height.

22. A semiconductor device having a hollow structure comprising:

a substrate on which a wiring layer is formed;

a low-dielectric layer having a porosity of 6% to 25%, said low-dielectric layer having vias and trenches formed therethrough and having voids between adjacent vias;

a contact layer of copper with which the vias and trenches are filled, said contact layer is in contact with the wiring layer and an upper surface of the contact layer is exposed from the dielectric layer.

23. The semiconductor device according to Claim 22, wherein the low-dielectric layer having voids has a dielectric constant of 2.3 or less.

24. The semiconductor device according to Claim 22, wherein the low-dielectric layer and the contact layer are laminated multiple times.

25. The semiconductor device according to Claim 22, wherein the voids are air gaps, and the vias and the air gaps are substantially of equal height.

26. The semiconductor device according to Claim 22, wherein the material of the low-dielectric layer has a dielectric constant of 2.9 or less.

27. The semiconductor device according to Claim 22, further comprising an etch stop layer between the first low-dielectric layer and the second low-dielectric layer.